INTEGRATED CIRCUIT TESTING METHODS

USING WELL BIAS MODIFICATION

Abstract

Methods for testing a semiconductor circuit (10) including testing the circuit and modifying a well bias (14, 18) of the circuit during testing. The methods improve the resolution of voltage-based and IDDQ testing and diagnosis by modifying well bias during testing. In addition, the methods provide more efficient stresses during stress testing. The methods apply to ICs where the semiconductor well (wells and/or substrates) are wired separately from the chip VDD and GND, allowing for external control (40) of the well potentials during test. In general, the methods rely on using the well bias to change transistor threshold voltages.

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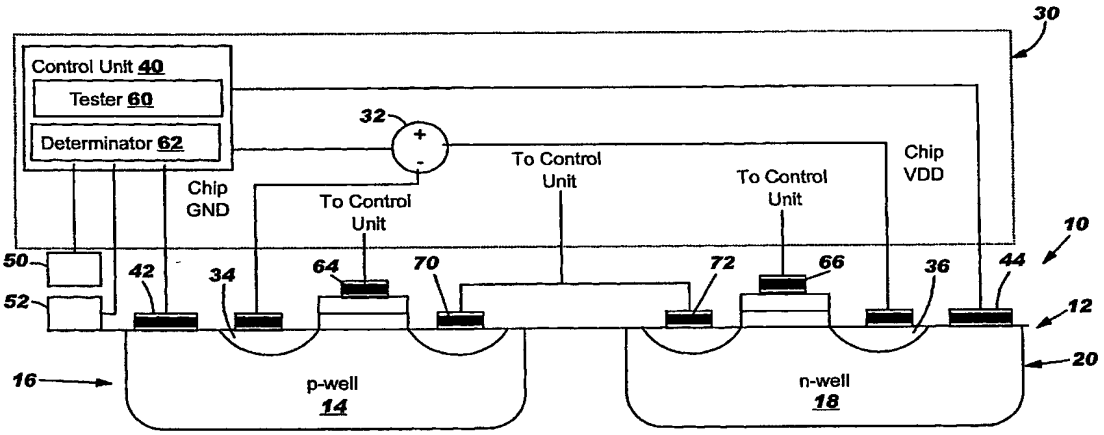

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